IN THE CLAIMS

What is claimed is:

1. A method for making a semiconductor device comprising:

forming a dielectric layer on a substrate;

forming a metal layer on the dielectric layer;

forming on the metal layer a masking layer that has first and second sides; and then

lining the first and second sides of the masking layer with a sacrificial layer.

2. The method of claim 1 wherein the dielectric layer comprises a high-k gate dielectric layer.

3. The method of claim 2 wherein the high-k gate dielectric layer comprises a material that is selected from the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate.

4. The method of claim 1 wherein the metal layer comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, a metal carbide, ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide.

5. The method of claim 1 wherein the metal layer is between about 25 and about 300 angstroms thick and has a workfunction that is between about 3.9 eV and about 4.2 eV.

6. The method of claim 1 wherein the metal layer is between about 25 and about 300 angstroms thick and has a workfunction that is between about 4.9 eV and about 5.2 eV.

7. The method of claim 1 wherein:

the masking layer comprises polysilicon;

the sacrificial layer comprises a material that is selected from the group consisting of silicon nitride, a carbon doped silicon nitride, and silicon dioxide; and

the first and second sides of the masking layer are lined with the sacrificial layer by depositing the sacrificial layer onto the metal layer, and onto the first and second sides of the masking layer, then applying an anisotropic plasma dry etch process to remove the sacrificial layer from the metal layer.

8. The method of claim 1 further comprising etching the metal layer and the dielectric layer after lining the first and second sides of the masking layer with the sacrificial layer, and removing the sacrificial layer after the metal layer is etched.

9. The method of claim 8 wherein:

the metal layer is etched by applying a plasma dry etch process to etch a first part of the metal layer, and applying a wet etch process to etch a second part of the metal layer;

a wet etch process is applied to etch the dielectric layer; and

a wet etch process is applied to remove the sacrificial layer.

10. A method for making a semiconductor device comprising:

forming a dielectric layer on a substrate;

forming a first metal layer on a first part of the dielectric layer, leaving a second part of the dielectric layer exposed;

forming a second metal layer on the first metal layer and on the second part of the dielectric layer;

forming on the second metal layer a masking layer that has first and second sides; and then

lining the first and second sides of the masking layer with a sacrificial layer.

11. The method of claim 10 wherein the dielectric layer comprises a high-k gate dielectric layer, the first metal layer comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and the second metal layer comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide.

12. The method of claim 10 wherein the dielectric layer comprises a high-k gate dielectric layer, the first metal layer comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide, and the second metal layer comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide.

13. The method of claim 10 wherein the first and second metal layers are each between about 25 and about 300 angstroms thick, the first metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV, and the second metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV.

14. The method of claim 10 wherein the first and second metal layers are each between about 25 and about 300 angstroms thick, the first metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV, and the second metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV.

15. The method of claim 10 wherein:

the masking layer comprises polysilicon;

the sacrificial layer comprises a material that is selected from the group consisting of silicon nitride, a carbon doped silicon nitride, and silicon dioxide; and

the first and second sides of the masking layer are lined with the sacrificial layer by depositing the sacrificial layer onto the second metal layer, and onto the first and second sides of the masking layer, then applying an anisotropic plasma dry etch process to remove the sacrificial layer from the second metal layer.

16. The method of claim 10 further comprising etching the second metal layer, the first metal layer, and the dielectric layer after lining the first and second sides of the masking layer with the sacrificial layer, and removing the sacrificial layer after the second metal layer and the first metal layer are etched.

17. The method of claim 16 wherein:

the second metal layer and the first metal layer are etched by applying a plasma dry etch process to etch a first part of the second metal layer and a first part of the first metal layer, and applying a wet etch process to etch a second part of the second metal layer and a second part of the first metal layer;

a wet etch process is applied to etch the dielectric layer; and

a wet etch process is applied to remove the sacrificial layer.

18. A method for making a semiconductor device comprising:

forming a high-k gate dielectric layer on a substrate;

forming a first metal layer on the high-k gate dielectric layer;

removing part of the first metal layer;

forming a second metal layer on the first metal layer and on the high-k gate dielectric layer, a first part of the second metal layer covering the remaining part of the first metal layer and a second part of the second metal layer covering the high-k gate dielectric layer;

forming a polysilicon layer on the second metal layer;

removing part of the polysilicon layer to generate a patterned polysilicon layer that has first and second sides, and to expose a third part of the second metal layer; and

lining the first and second sides of the patterned polysilicon layer with a sacrificial layer.

19. The method of claim 18 wherein:

the sacrificial layer comprises a material that is selected from the group consisting of silicon nitride, a carbon doped silicon nitride, and silicon dioxide;

the first and second sides of the patterned polysilicon layer are lined with the sacrificial layer by depositing the sacrificial layer onto the second metal layer, and onto the first and second sides of the patterned polysilicon layer, then applying an anisotropic plasma dry etch process to remove the sacrificial layer from the second metal layer; and further comprising:

removing the exposed third part of the second metal layer and the underlying part of the first metal layer after lining the first and second sides of the patterned polysilicon layer with the sacrificial layer; and

removing the sacrificial layer after the exposed third part of the second metal layer and the underlying part of the first metal layer are removed.